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Title:

IMPROVED MEMORY CELL CAPACITOR STRUCTURE AND METHOD OF FORMATION

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BACKGROUND OF THE INVENTION

The present invention relates to the design and manufacture of dynamic random access memory (DRAM) devices and particularly to a method of fabrication and resulting structure of Metal-Insulator-Metal (MIM) capacitors which have reduced capacitor current leakage.

DESCRIPTION OF RELATED ART

The memory cells of modern dynamic random access memory (DRAM) devices contain two main components: a field effect transistor and a capacitor. High memory capacity DRAM cells typically employ a non-planar capacitor structure. Two basic non-planar capacitor structures are currently popular: the trench capacitor and the stacked capacitor. Their fabrication typically require considerably more masking, deposition and etching steps than for planar capacitor structures. The MIM structure can be used for either type of non-planar capacitor. Most manufacturers of 4-megabit or larger DRAMS utilize a non-planar capacitor. A non-planar capacitor structure with a Metal-Insulator-Metal (MIM) structure provides higher capacitance and hence makes it possible to produce higher density memories.

The top and bottom conducting layers, also referred to as electrodes or plates, of a MIM capacitor are typically patterned from individual layers of various metal materials and sandwich a dielectric layer. Both the top and bottom conducting layers are often made with the same material; however this is not a requirement. Increasing the dielectric constant for the dielectric layer allows greater charge to be stored in a cell capacitor for a given dielectric thickness. To this end Tantalum Oxide and Barium Strontium Titanate

(BST) have been described as useful dielectric materials, as they both have high dielectric constants, also referred to as high permittivity or large capacitance. See, U.S. Patent No. 5,142,438; Benjamin Chih-ming Lai and Joseph Ya-min Lee, Leakage Current Mechanism of Metal-Ta_2O_5-Metal Capacitors for Memory Device Applications, 146 Journal of the Electrochemical Society 262 (1999); Tomonori Aoyama, Soichi Yamazaki, and Keitaro Imai, Ultrathin Ta_2O_5 Film Capacitor with Ru Bottom Electrode, 145 Journal of the Electrochemical Society 2961 (1998); and G.W. Dietz, M. Schumacher, R. Waser, S.K. Streifffer, C. Basceri, and A.I. Kingon, Leakage Currents in $Ba_{0.7}Sr_{0.3}TiO_3$ Thin Films for Ultra-density Dynamic Random Access Memories, 82 Journal of Applied Physics 2359 (1997). The higher the permittivity or dielectric capacitance of the dielectric material, the more charge can be stored by the capacitor. In addition a smaller capacitor with a higher permittivity can also store the same amount of charge as a larger capacitor with a lower permittivity.

As discussed in cited materials, when a Tantalum Oxide or BST film is used as a dielectric layer in a stacked capacitor structure an oxygen annealing process must be employed after dielectric film deposition to reduce the high current leakage. As formed the dielectric layer contains defects such as oxygen vacancies. The oxygen anneal performed before depositing the top conducting layer fills oxygen vacancies in the dielectric layer. The cited references teach that current leakage from a MIM stacked capacitor is significantly reduced after an oxygen anneal is performed on the dielectric layer. However, during subsequent wafer fabrication, the dielectric layer develops oxygen vacancies which contribute to capacitor current leakage. For example a Tantalum Oxide film could react

with Chlorine or Fluorine ions used during a dry etch, especially if the etch is formed at temperatures greater than 200 degrees Celsius.

What is needed is a DRAM cell which further reduces the current leakage from a capacitor.

SUMMARY OF THE INVENTION

The present invention is directed to an improved capacitor for a semiconductor device, especially a MIM Dynamic Random Access Memory (DRAM) device, which has a reduced current leakage. The invention also relates to a method of fabricating a capacitor, e.g., a MIM capacitor, having reduced current leakage. The capacitor is constructed with a bottom and top conducting layer sandwiching a dielectric layer. The bottom conducting layer could be a metal, metal alloy, conducting metal oxide, or metal nitride. It is preferred that it is not permeable to oxygen. The top conducting layer is a member of the noble metal group or is a conducting metal oxide, and should be permeable to oxygen. The dielectric layer is a dielectric metal oxide with a dielectric constant between 7 and 300 and may, for example, be a Tantalum Oxide or BST film.

The method of the invention includes the following steps. The bottom conducting layer is deposited and patterned then the dielectric layer is deposited over the bottom conducting layer. An anneal is performed on the exposed dielectric layer surface with an oxidizing compound gas. The top conducting layer is then deposited over the dielectric layer. The method of the invention improves the capacitor's charge retention through the use of an oxidizing compound gas anneal after the top conducting layer is formed. The

oxygen ions pass through the oxygen permeable top conducting layer and are diffused into the dielectric layer and fill oxygen vacancies created in the dielectric layer during the deposition and patterning of the top conducting layer which reduces current leakage through the dielectric layer.

The second anneal may be performed for a period of between 10 seconds and 60 minutes at a temperature of between 300 and 800 degrees Celsius and at a pressure of 1 to 760 torr. Also disclosed are preferred compounds for use as the top and bottom conducting layers of the stacked capacitor and for use in the anneal step. The anneal step can also be enhanced with plasma, remote plasma, or ultraviolet light.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other advantages and features of the invention will be more readily understood from the following detailed description of the invention which is provided in connection with the accompanying drawings.

FIG. 1 is a cross-sectional view of a stacked capacitor of a dynamic random access memory (DRAM) array which is fabricated in accordance with the invention.

FIG. 2 is a graphical comparison of the current leakage of a stacked capacitor with a top conducting layer of Platinum (Pt), a bottom conducting layer of Tungsten Nitride (WN_x), a dielectric layer of Tantalum Pentoxide (Ta_2O_5) before and after a second anneal step performed on the top conducting layer.

FIG. 3 is a graphical comparison of the current leakage of four stacked capacitors with a top and bottom conducting layer of Platinum (Pt) and a dielectric layer of Barium

Strontium Titanate (BST) after several different anneal steps were performed on the four capacitors.

FIG. 4 illustrates a processor based system employing an improved dynamic random access memory (DRAM) device with a capacitor fabricated in accordance with the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to FIG. 1, a cross-sectional portion of a dynamic random access memory (DRAM) array 10 of a stacked capacitor design is depicted after a final insulating layer 48 is applied to the capacitor cell. The capacitor cell is built on a substrate 12, which also contains a gate oxide region 14 and a pair of source/drain diffusion regions 22. A pair of gate stacks 29, 31 are formed by an oxide layer 50, doped poly-silicon layer 18, a silicide region 56, and an insulating cap layer 55. The doped poly-silicon layer 18 of gate stack 29 acts as a word line for the DRAM device. In this embodiment stacked gate 29 and diffusion regions 22, form an access transistor for a memory cell which includes the access transistor and a capacitor. Electrically insulated sidewall spacers 54 are formed on the sidewalls of the gate stacks 29, 31. Also shown are a pair of electrically conductive plugs 62, 63 extending through to the respective diffusion regions 22. An insulating layer 44 of Borophosphosilicate glass (BPSG) or other suitable insulation material is provided over the stacked gates 29, 31 and substrate 12 and the plugs 62, 63 are formed in this insulating layer.

An overlying insulating layer 46 of BPSG or other suitable insulation material layer is provided over insulating layer 44, and includes an opening 30 through to conductive plug 63. Another opening is formed in layer 46 down to plug 62 and is filled with a conductor 61. A capacitor is formed in opening 30 and includes a bottom conducting layer 34, a dielectric layer 36, and a top conducting layer 38. After the bottom conducting layer 34 and dielectric layer 36 are deposited a first anneal is performed on the capacitor prior to depositing the top conducting layer 38.

The dielectric layer 36 anneal is performed with an oxidizing gas, for between 10 seconds and 60 minutes, preferably between 10 seconds to 30 minutes, at a temperature of between 300 and 800 degrees Celsius, preferably between 400 and 650 degrees Celsius, and at a pressure of between 1 to 760 torr, preferably 2 to 660 torr. Suitable oxidizing gas compounds for use in the anneal step include: Oxygen (O_2), Ozone (O_3), Nitrous Oxide (N_2O), Nitric Oxide (NO), and water vapor (H_2O). These gases can be introduced individually into an oxidizing chamber or can be produced from reactions of other materials in the oxidization chamber. The oxidizing gas could also be a mixture of one or more these gases with an inert gas such as Argon (Ar), Helium (He), Nitrogen (N_2), or other compound mixtures which produces reacting oxygen ions. The introduction of these materials during the dielectric anneal may also be enhanced by plasma, remote plasma, or ultraviolet light. The flow rate of the gas should be between 0.01 and 10 liters per minute (l/min). A typical prior art process for the dielectric anneal on a dielectric layer of Tantalum Oxide is Ozone gas for 3 minutes, at a temperature of 475 degrees Celsius, and at a pressure of 4.0 torr. A typical prior art process for the dielectric anneal on a dielectric

layer of Barium Strontium Titanate (BST) is Ozone gas, enhanced with plasma for 3 minutes at a temperature of 475 degrees Celsius at a pressure of 4.0 torr.

After the dielectric anneal, the top conducting layer 38 is deposited patterned, and etched such that capacitors are formed in opening 30 on the wafer 12. An anneal in the presence of oxygen after a dielectric layer 36 of Tantalum Oxide or BST film has been deposited replenishes much of the oxygen lost from the dielectric layer 36 during the layer's deposition.

The present invention further improves the dielectric property of the dielectric layer 36 by adding an oxidizing gas anneal (second anneal) which fills the oxygen voids created in the dielectric layer 36 after the top conducting layer 38 is deposited. The second anneal should be performed with an oxidizing gas, for between 10 seconds and 60 minutes, preferably between 10 seconds to 30 minutes, at a temperature of between 300 and 800 degrees Celsius, preferably between 400 and 750 degrees Celsius, and at a pressure of between 1 to 760 torr, preferably 2 to 660 torr. Suitable oxidizing gas compounds for use in the second anneal step include: Oxygen (O_2), Ozone (O_3), Nitrous Oxide (N_2O), Nitric Oxide (NO), and water vapor (H_2O). These gases can be introduced individually into an oxidizing chamber or can be produced from reactions of other materials in the oxidization chamber. The oxidizing gas could also be a mixture of one or more these gases with an inert gas such as Argon (Ar), Helium (He), Nitrogen (N_2), or other compound mixtures which produces reacting oxygen ions. The introduction of these materials during the second anneal may also be enhanced by plasma, remote plasma, or ultraviolet light. The flow rate of the gas is between 0.01 and 10 liters per minute (l/min).

After the capacitor cell is formed the substrate 12 is then coated with insulating layer 48 of BPSG or other suitable insulation material. Also shown in Figure 1 is an electrically conductive bit line 70 which connects to active region 22 through conductive plugs 61 and 62 and word line 18, which is also the gate of access transistor 29. The array and peripheral circuitry are then completed using techniques well-known in the art.

A first preferred embodiment for a stacked capacitor cell has a bottom conducting layer 34 and top conducting layer 38 formed from a noble metal, which resists oxidization. The bottom conducting layer 34 can be permeable to oxygen, but it should resist oxidization. However, if the bottom layer 34 is permeable to oxygen, an oxygen barrier layer may be needed between the bottom layer 34 and plug 63 to prevent layer 63 made of poly-silicon from oxidizing during the anneal process. The bottom conducting layer 34 and top conducting layer 38 can be of different materials. The bottom conducting layer 34 can be a metal, metal alloy, conducting metal oxide, or metal nitride. The bottom conducting layer is formed of compounds selected from the group consisting of: Platinum (Pt), Platinum Rhodium (PtRh), Platinum Iridium (PtIr), Ruthenium, Ruthenium Oxide (RuO_2), Rhodium Oxide (RhO_2), Chromium Oxide (CrO_2), Molybdenum Oxide (MoO_2), Rhemium Oxide (ReO_3), Iridium Oxide (IrO_2), Titanium Oxides (TiO_1 or TiO_2), Vanadium Oxides (VO_1 or VO_2), Niobium Oxides (NbO_1 or NbO_2), and Tungsten Nitride (WNx, WN, or W_2N). The bottom conducting layer 34 is preferably formed from Platinum (Pt), a Platinum alloy, such as Platinum Rhodium (PtRh) or Platinum Iridium (PtIr), or Tungsten Nitride (WNx, WN, or W_2N).

The dielectric layer 36 should be an metal dielectric oxide with a dielectric constant between 7 and 300. The dielectric layer 36 is formed from compounds selected from the group consisting of: Tantalum Oxide, Tantalum Pentoxide (Ta_2O_5), Barium Strontium Titanate (BST), Aluminum Oxide (Al_2O_3), Zirconium Oxide (ZrO_2), Praseodymium Oxide (PrO_2), Tungsten Oxide (WO_3), Niobium Pentoxide (Nb_2O_5), Strontium Bismuth Tantalate (SBT), Hafnium Oxide (HfO_2), Hafnium Silicate, Lanthanum Oxide (La_2O_3), Yttrium Oxide (Y_2O_3) and Zirconium Silicate. The dielectric layer 36 is preferably formed from Tantalum Pentoxide (Ta_2O_5), Barium Strontium Titanate (BST), Strontium Bismuth Tantalate (SBT), Aluminum Oxide (Al_2O_3), Zirconium Oxide (ZrO_2) or Hafnium Oxide (HfO_2). If the dielectric layer 36, is Tantalum Oxide, it could be amorphous or crystalline. If it is amorphous, it could be crystallized during the annealing process to achieve a higher dielectric permittivity. For example Tantalum Oxide amorphous has a dielectric constant between 18 and 25; however crystalline Tantalum Oxide has a dielectric constant 40. Prior to depositing the top conducting layer 38, the first anneal described above is performed.

The top conducting layer 38 must be a non-oxidizing metal, a noble metal, or a conducting metal oxide permeable to oxygen to allow oxidizing gas used in the second anneal step after the top conducting layer 38 is patterned to pass through the top conducting layer 38 and into the dielectric layer 36. The top conducting layer 38 is formed of compounds selected from the group consisting of: Platinum (Pt), Platinum Rhodium (PtRh) or Platinum Iridium (PtIr), Ruthenium, Ruthenium Oxide (RuO_2), Rhodium Oxide (RhO_2), Chromium Oxide (CrO_2), Molybdenum Oxide (MoO_2), Rhemium Oxide (ReO_3), Iridium Oxide (IrO_2), Titanium Oxides (TiO_1 or TiO_2), Vanadium Oxides (VO_1 or VO_2), and Niobium Oxides (NbO_1 or NbO_2). The top

conducting layer 38 is preferably formed from Platinum (Pt) or a Platinum alloy, such as Platinum Rhodium (PtRh) or Platinum Iridium (PtIr).

A second preferred embodiment for a stacked capacitor cell has a bottom 34 and top 38 conducting layer formed of a compound selected from the group consisting of: Platinum, Platinum Rhodium (PtRh), or Platinum Iridium (PtIr) and a dielectric layer 36 formed of a layer of either Tantalum Oxide or Barium Strontium Titanate (BST).

A third preferred embodiment of a stacked capacitor cell has a bottom conducting layer 34 formed of Tungsten Nitride (WNx, WN, or W_2N), a dielectric layer 36 formed of Aluminum Oxide (Al_2O_3), and a top conducting layer 38 formed of a compound selected from the group consisting of: Platinum, Platinum Rhodium (PtRh), or Platinum Iridium (PtIr).

FIG. 2 is a comparison of the current leakage of a stacked capacitor with a Platinum (Pt) top conducting layer 38 and a Tungsten Nitride (WN_x) bottom conducting layer 34 and a Tantalum Pentoxide (Ta_2O_5) dielectric layer 36 before and after the top conducting layer 38 is annealed. The samples were constructed with a prior art first anneal on the dielectric layer 36 of Ozone gas, enhanced with plasma for 3 minutes at a temperature of 475 degrees Celsius at a pressure of 4.0 torr. After depositing the top conducting layer 38, a second oxidizing gas anneal, in accordance with the present invention, was performed for 3 minutes at a temperature of 475 degrees Celsius at a pressure of 4 torr, with an oxygen and ozone mixture. The capacitance of the capacitor, biased at 1 volt, was then measured after it had cooled to a temperature of 85 degrees Celsius. The x-axis shows the capacitance in capacitance per units/area (femto-Farad per micrometer squared (fF/μ^2)).

The y-axis shows the leakage current density in current per area (amperes per centimeter squared (A/cm^2)). As the diagram shows the capacitance of the capacitor before and after the anneal was approximately 21 (fF/μ^2); however the current leakage density after the anneal was reduced by a factor of approximately 10.

FIG. 3 is a comparison of the current leakage between a stacked capacitor with a Platinum (Pt) top 38 and bottom 34 conducting layer and a Barium Strontium Titanate (BST) dielectric layer. The four samples were each constructed with a prior art first anneal on the dielectric layer 36 of Ozone gas, enhanced with plasma for 3 minutes at a temperature of 475 degrees Celsius at a pressure of 4.0 torr. A second anneal step, in accordance with the present invention, was performed on four samples after the top conducting layer 38 was deposited, at a temperature of 550 degrees Celsius and a pressure of 660 torr. One capacitor was subject to Oxygen gas anneals of 10 minutes, one capacitor was subject to Oxygen gas anneals for 30 minutes, and one with Nitrogen gas for 10 minutes and one with Nitrogen gas for 30 minutes. The capacitance of the capacitors, biased at 1 volt, was then measured after anneal. The wafer was heated to 85° C during measurement to simulate stringent real DRAM application conditions.

The x-axis shows the capacitance in capacitance per unit area (femto-Farad per micrometer squared (fF/μ^2)). The y-axis shows the leakage current density in current per unit area (amperes per centimeter squared (A/cm^2)). As the diagram shows the current leakage density for capacitors annealed with Nitrogen gas for both the 10 and 30 minute anneals produced a current leakage that exceed 2000 (A/cm^2), which was the maximum level the machine could detect. As expected, the capacitors annealed with Nitrogen gas,

which is an inert non-oxidizing gas, produced no current leakage reduction. However, the two capacitors which were annealed with Oxygen gas for 10 and 30 minute anneals had current leakage density reductions by a factor of 10 to 100 times of the Nitrogen gas samples. Thus the test shows that performing an anneal step with an oxidizing gas after the top conducting layer 38 is formed substantially reduced capacitor current leakage.

FIG. 4 illustrates a typical processor based system 102, including a DRAM memory device 108 containing a stacked capacitor fabricated according to the present invention as illustrated in FIG. 1 and described above. A processor based system, such as a computer system 102, generally comprises a central processing unit (CPU) 112, for example a microprocessor, that communicates with one or more input/output(I/O) devices 104, 106 over a bus 118. The computer system 102 also includes a read only memory device (ROM) 110 and may include peripheral devices such as floppy disk drive 114 and a CD ROM drive 116 which also communicates with the CPU 112 over the bus 118. DRAM device 108 preferably has a stacked capacitor which includes a top conducting layer anneal as previously described with reference to FIGS. 1-3.

While the invention has been illustrated and described in detail in the drawings and foregoing description, the above description and accompanying drawings are only illustrative of preferred embodiment which can achieve the features and advantages of the present invention. It is not intended that the invention be limited to the embodiments shown and described in detail herein. The invention is only limited by the scope of the following claims.